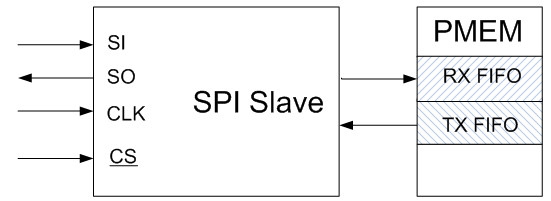
**SPISlave Module Description Document**

**1. Introduction**  
The SPI Slave module (hereinafter referred to as SPIS) has four signal lines: MISO, MOSI, CLK, and SS. A schematic of the communication connection can be found in the SPIM documentation.

The SPIS mode uses memory space as the transmit and receive buffer, each with a maximum size of 32,767 bytes. SPIS can access the PMEM side, which shares the same bus as UART. Therefore, SPIS and UART cannot both operate in PMEM mode simultaneously.

If the transmit buffer is empty and additional CLK pulses are received, the last byte of data will be repeatedly sent.

As a slave device, SPIS depends on the master device’s clock. After initialization, it will send 2 to 3 bytes of 0xFF before sending the actual data from the transmit buffer.

  
Figure 1 — SPIS buffer diagram

**2. Main Features**

  Maximum supported clock speed: 24 MHz.

  Supports four combinations of clock polarity and clock phase.

  Supports transmit and receive buffers up to 32,767 bytes in size.